AMENDMENT

IN THE CLAIMS:

Please add New Claims 35 – 45 so as to read as follows:

35. (New Claim) A shift register circuit, comprising:

a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;

a clock signal line transmitting a clock signal;

a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein at least one of the switching circuits electrically disconnects at least one of the plurality of latch circuits from the clock signal line at regular intervals;

potentials at nodes of the plurality of latch circuits vary in accordance with the pulse transferred;

the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits; and

in at least part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency lower than in a normal operation period;

wherein the frequency of the clock signal gradually increases in at least part of said period.

B1 cont

36. (New Claim) The shift register circuit according to Claim 35, wherein the frequency of the clock signal in said at least a part of the period is from 1/ 2 to 1/16 of a frequency of the clock signal in the normal operation period.

37. (New Claim) The shift register circuit according to Claim 35, wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and initializing an internal node of the latch circuit in response to the initialization signal.

B1 cont

38. (New Claim) The shift register circuit according to Claim 35, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.

39. (New Claim) The shift register circuit according to Claim 35, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.

40. (New Claim) The shift register circuit according to Claim 35, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit further comprises a level shifter changing the amplitude of the clock signal received from outside.

41. (New Claim) An image display device of active matrix type, comprising:
a plurality of pixels arranged in a matrix form;
a data signal line supplying video data to be written to one of the plurality of pixels;
a scan line for controlling the writing of the video data to one of the plurality of pixels;
a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and
a scan driver supplying a pulse signal to the scan line in synchronization with a timing signal;
at least one of the data driver and the scan driver comprising the shift register circuit according to claim 35.

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42. (New Claim) The image display device according to claim 41, wherein the data driver has the shift register circuit, and initializes the potential level at each internal node of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.

43. (New Claim) The image display device according to claim 41, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels are also formed.

44. (New Claim) The image display device according to claim 43, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.